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Virtual Multiprocessor: An Analyzable, High-Performance Microarchitecture for Real-Time Computing

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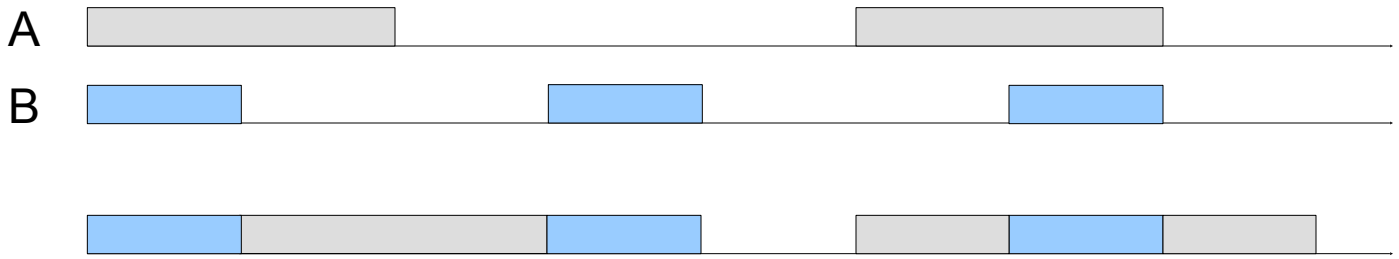
Embedded Processor Trends

- Inheriting desktop high-performance features
- Examples
  - ARM11: 8-stage pipeline, caches, dynamic br. pred.
  - Ubicom IP3023: 8 hardware threads
  - PowerPC 750: 2-way superscalar, OOO execution

Real-Time Systems and Analyzability

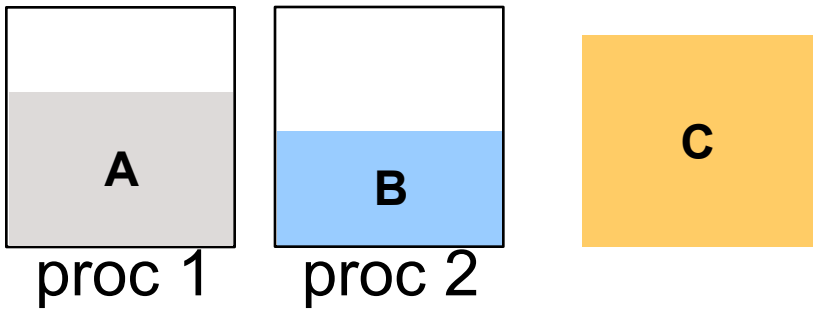


- Schedulability of task-set determined *a priori*
  - Requires worst-case execution times (WCET)
  - ∴ statically analyzable microarchitecture
- Dynamic microarchitecture features complicate real-time design

A trade-off between performance and analyzability

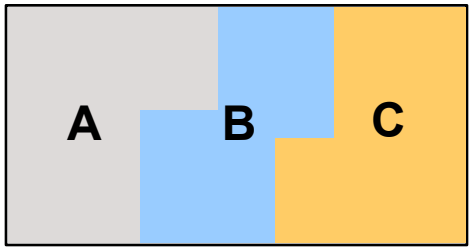
Multiple Simple Processors

+ Analyzable
+ Natural fit with real-time systems
− Rigid resource partitioning
− Higher cost/performance metric



Simultaneous Multithreading (SMT)

+ Flexible resource sharing
+ Better cost/performance metric
− Unanalyzable



SMT

Unanalyzability of SMT

- Violates single-task WCET assumption (tasks analyzed separately)
- Arbitrary periods → arbitrary overlap of tasks
- Dynamic interference

Cannot derive WCETs

→ Cannot perform schedulability

Real-Time Virtual Multiprocessor

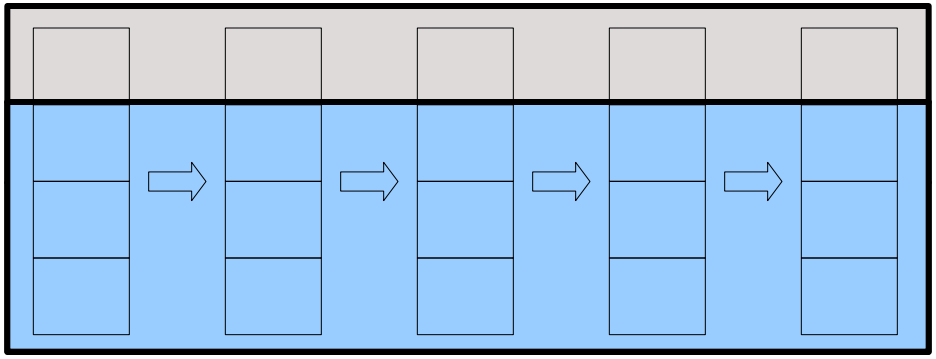
- Combine MP analyzability and SMT flexibility
- Key idea: **Interference-free multithreading**
  - SMT performance
  - WCET of each task independent of task-set
- RVMP substrate: two parts
  - Highly reconfigurable multithreaded superscalar
    - Space: multiple arbitrary interference-free partitions
    - Time: rapidly reconfigure partitions
  - Static schedule orchestrates partitioning

Big Picture

Co-design processor and real-time scheduling for analyzable high-performance

RVMP Architecture

- Superscalar "ways" are natural partitioning granularity
- Different-sized *virtual processors* carved out of single superscalar

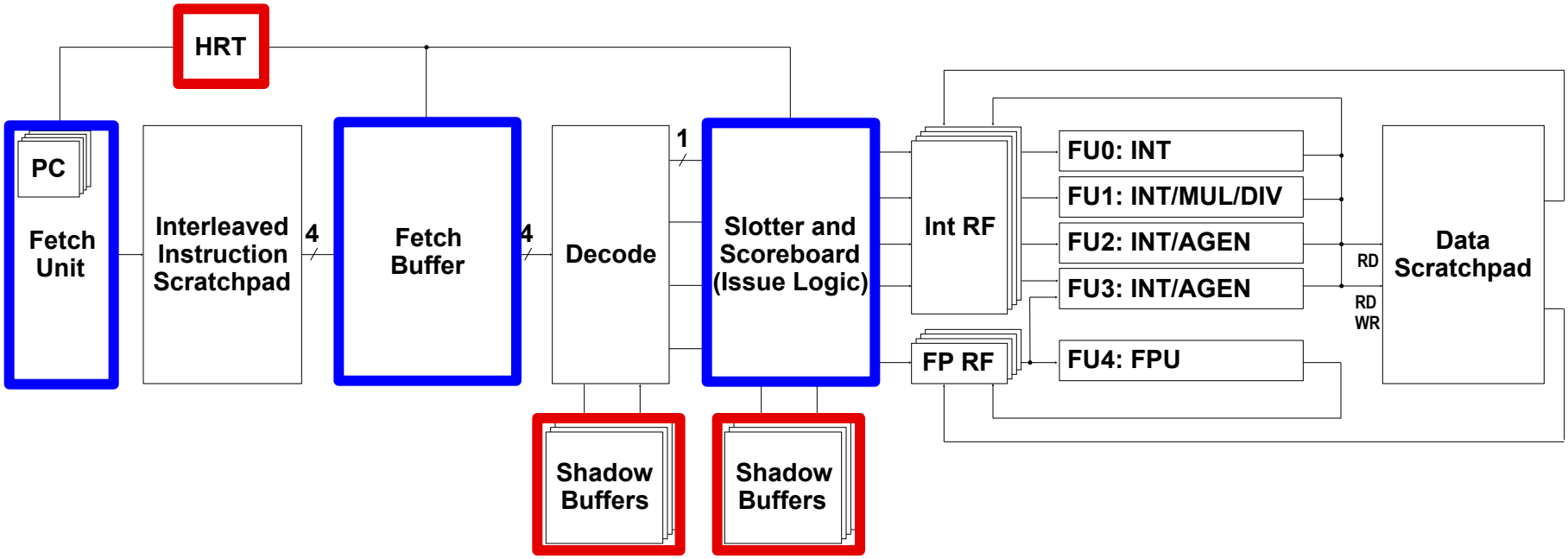


Processor Architecture

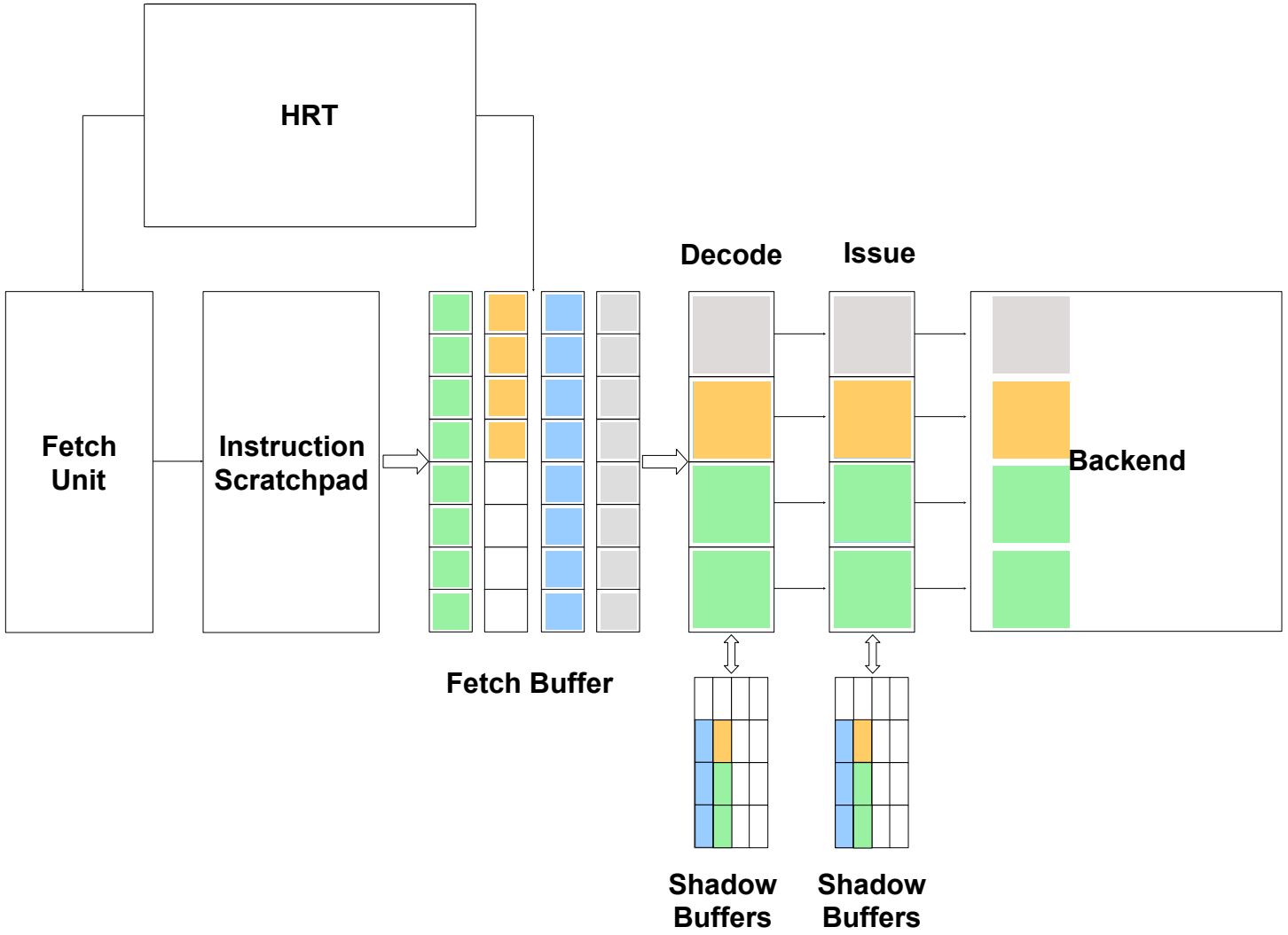
- Starting point
  - Alpha 21164: 4-way in-order superscalar
  - Ubicom IP3023: 8 hardware threads
    (4 in RVMP → 4 VPs)
- Simplifications for analyzability
  - In-order issue within VPs
  - Software-managed scratchpads
  - Static branch prediction

} Not limitations of RVMP!

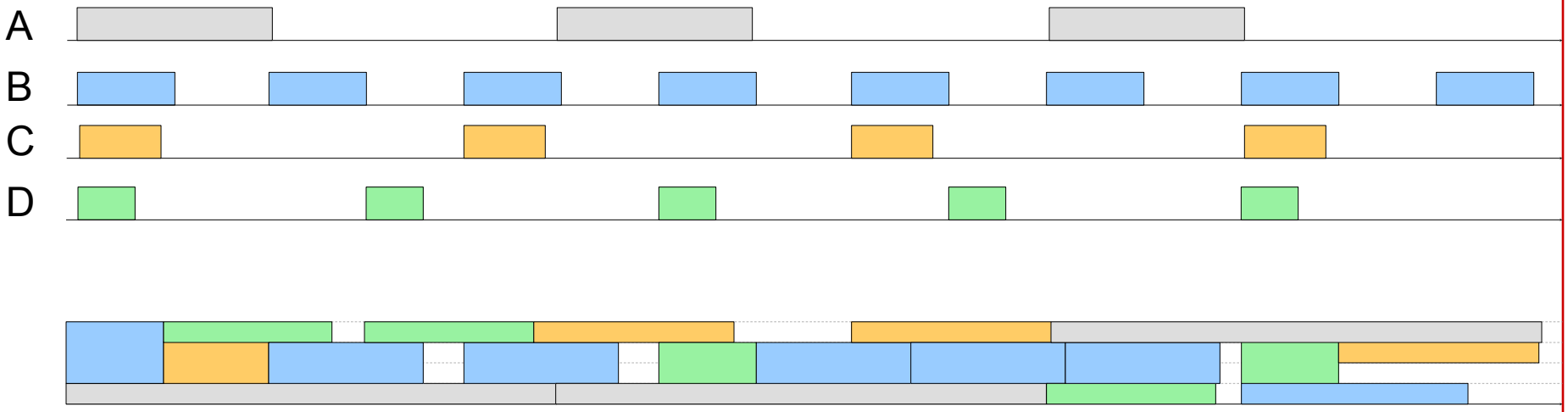
Processor Architecture



Instruction Fetch

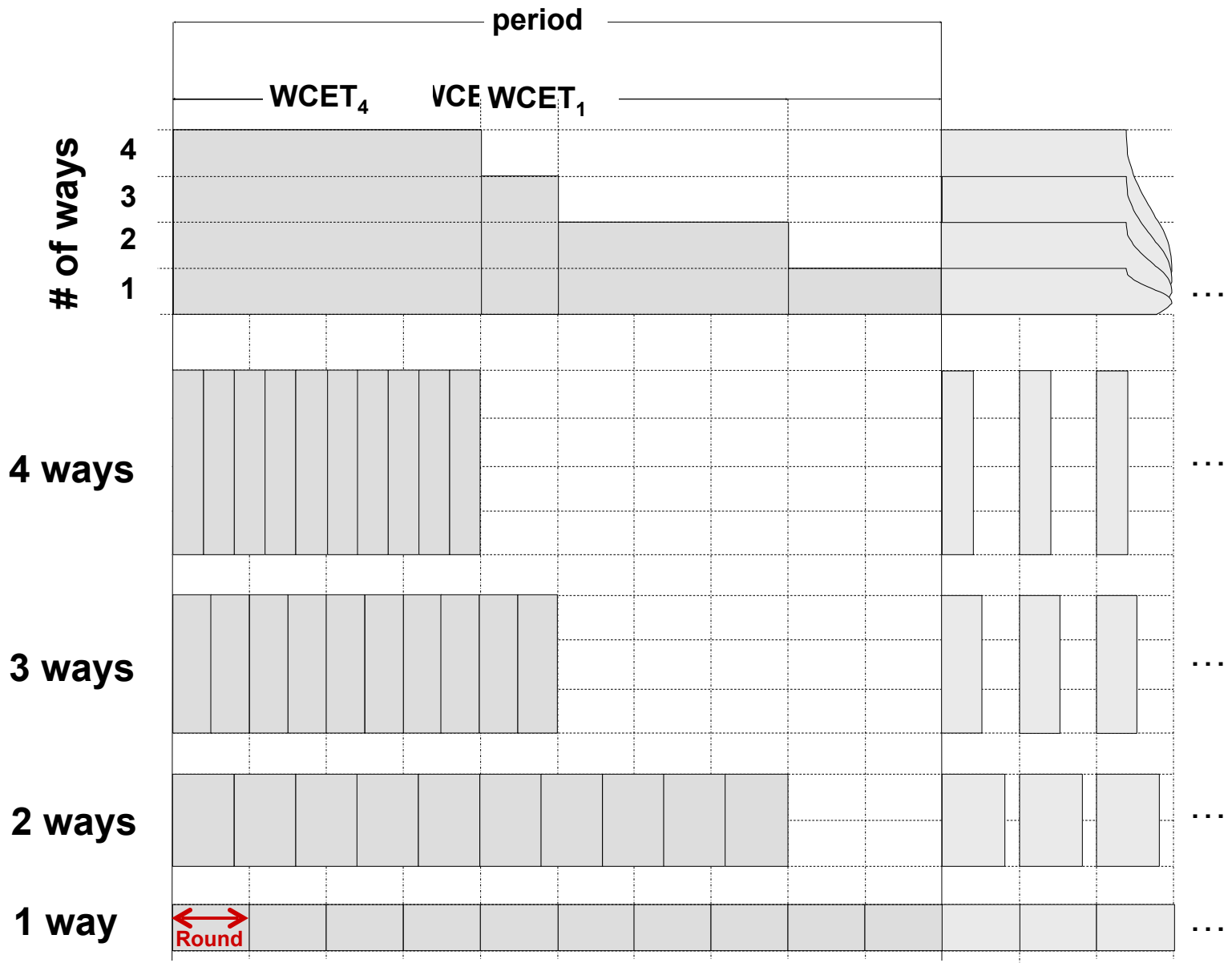


Real-Time Scheduling

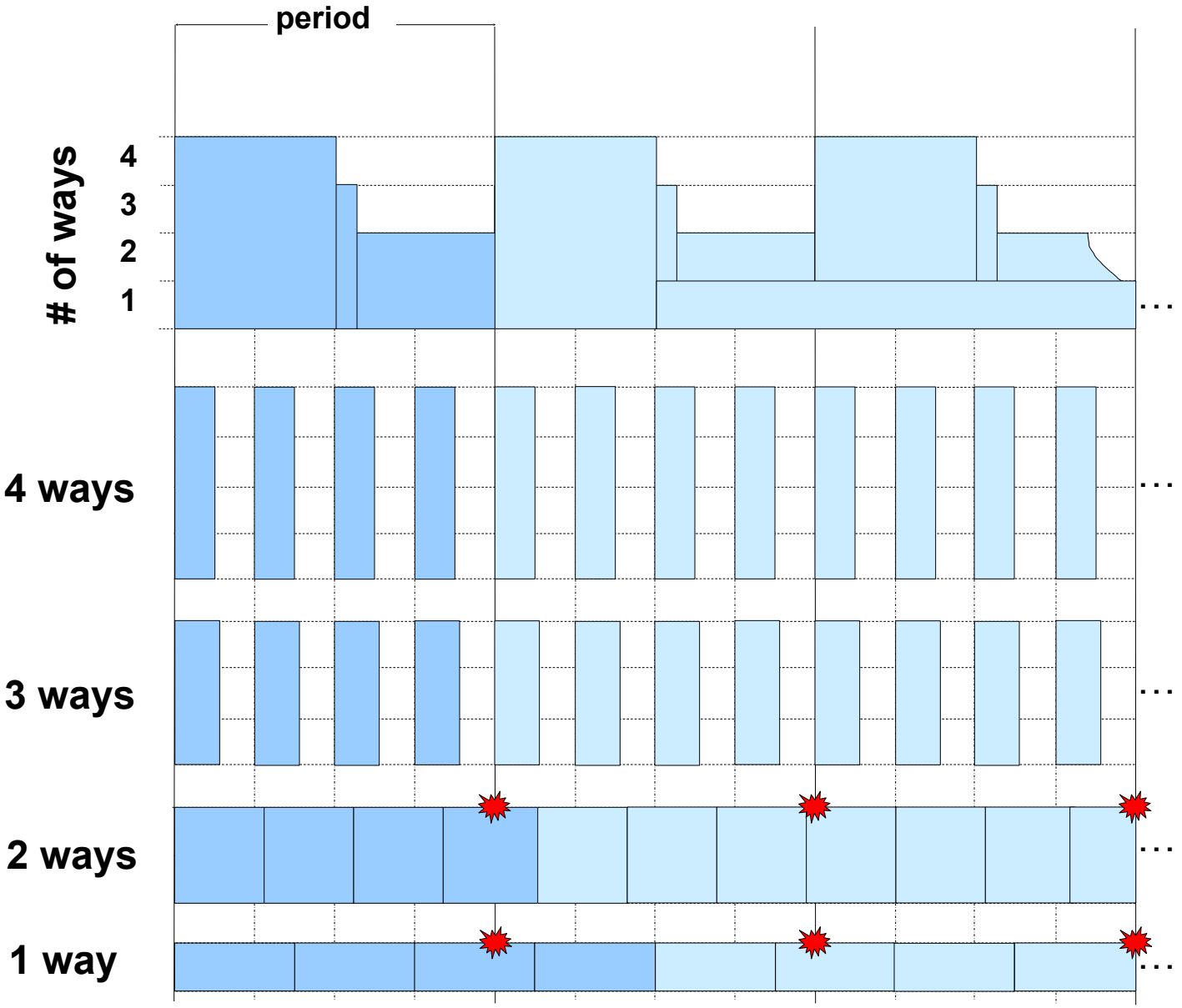


- Too complicated
  - Must schedule entire hyper-period
  - Overwhelming # of possible space/time schedules
  - High dedicated-storage cost for schedule

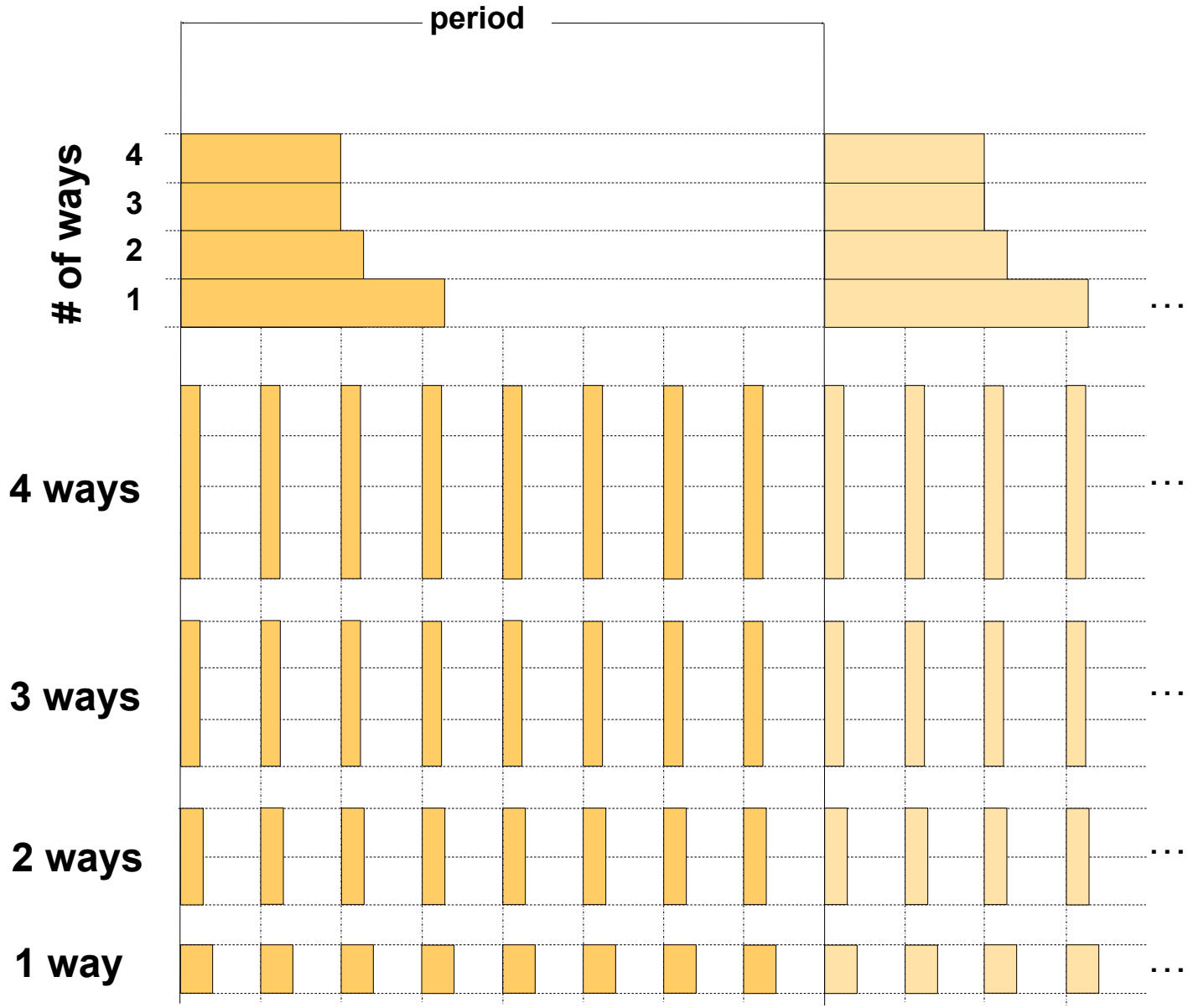
Task A


period
WCET4
WCET1
# of ways
4
3
2
1
4 ways
3 ways
2 ways
1 way
Round

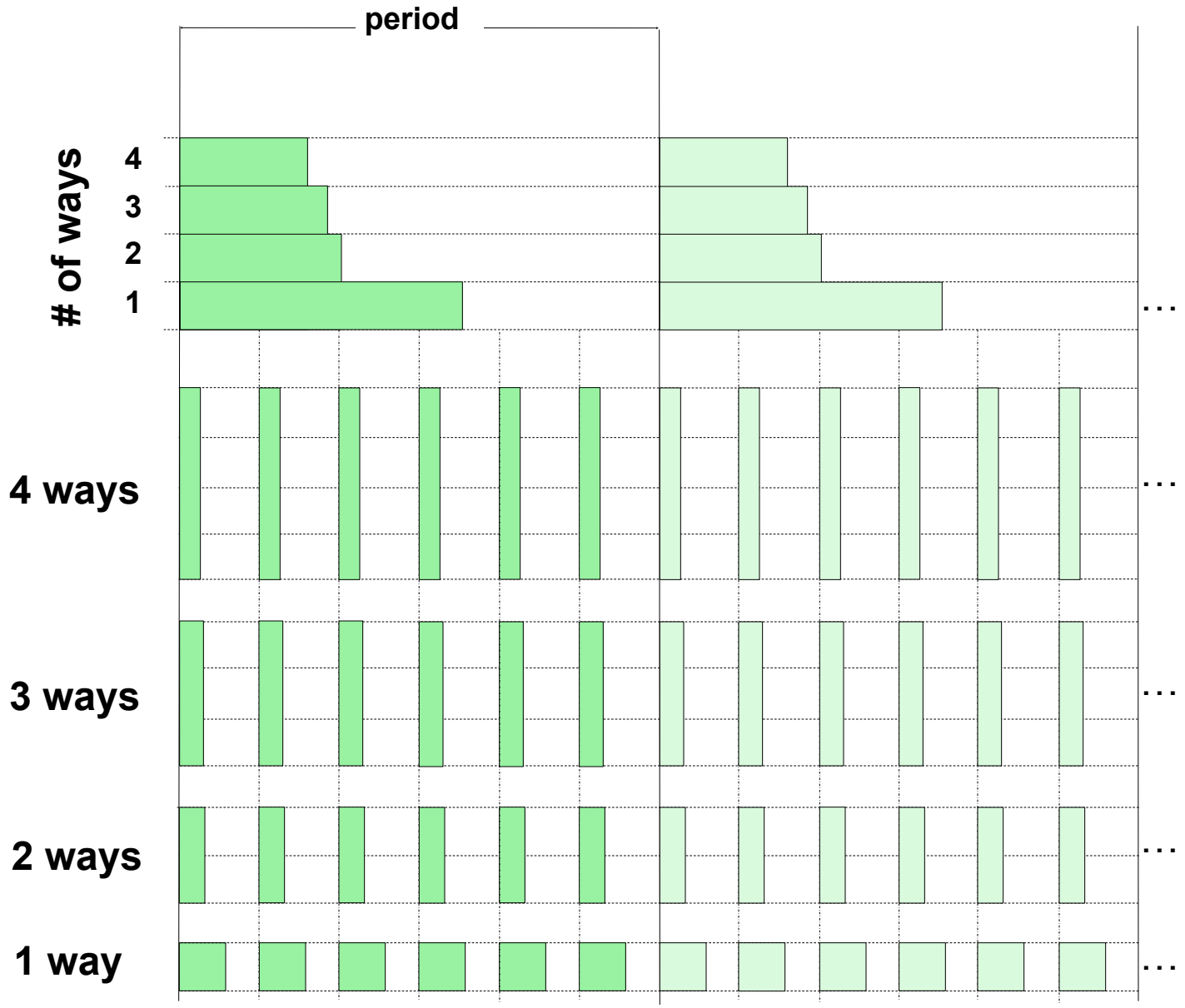
Task B

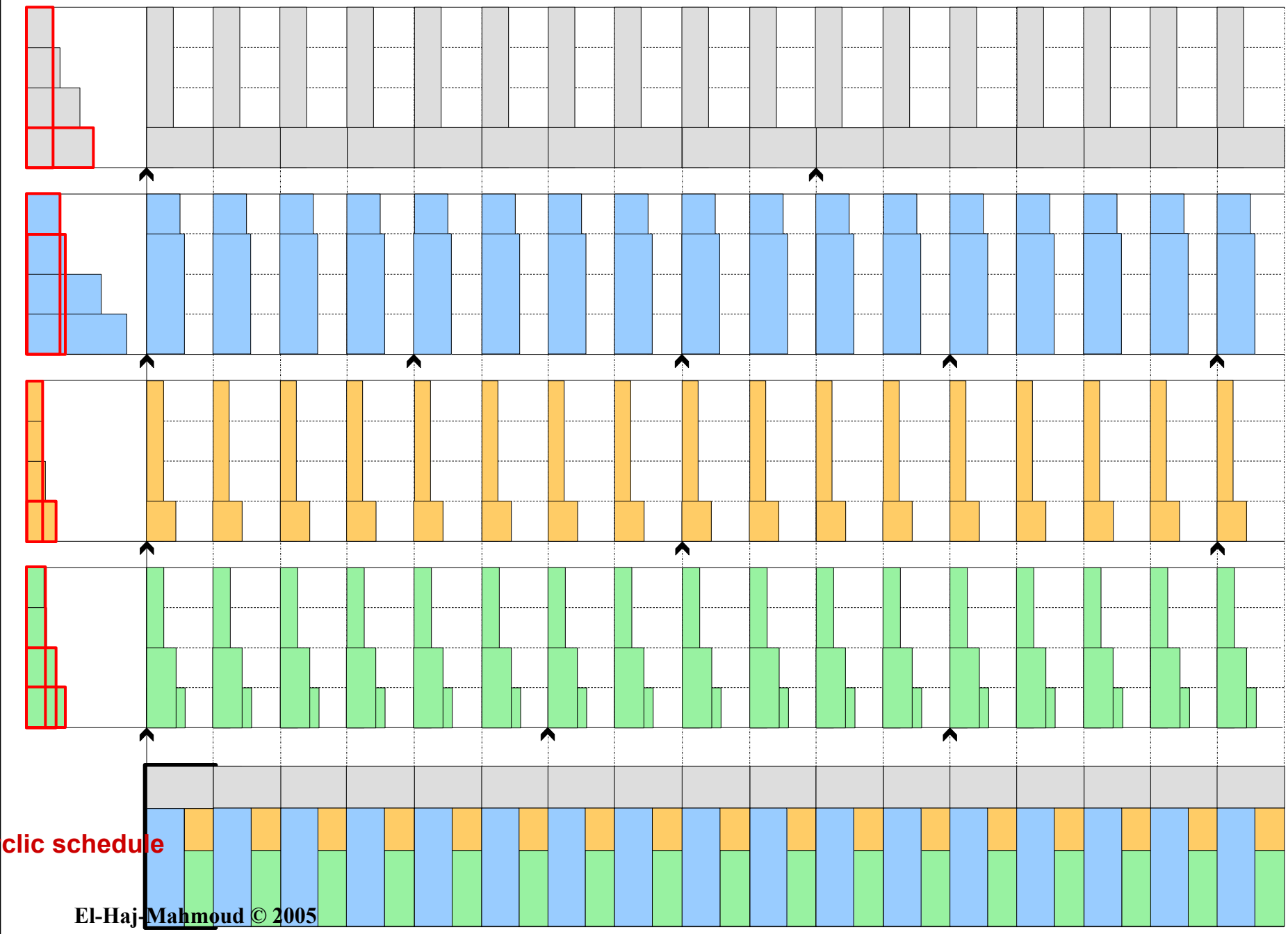


Task C

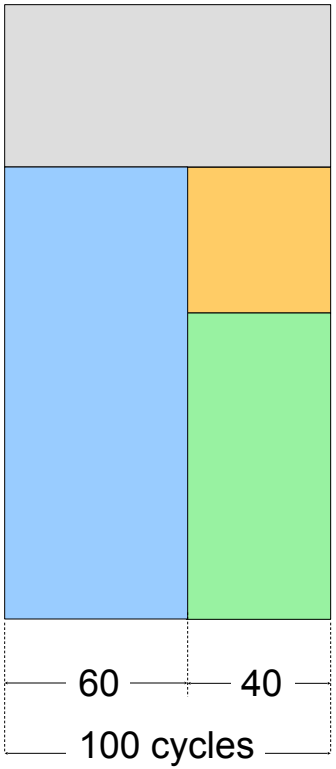


Task D

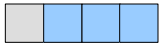
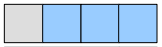
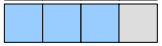
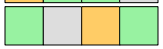




Interaction: Scheduling and Architecture



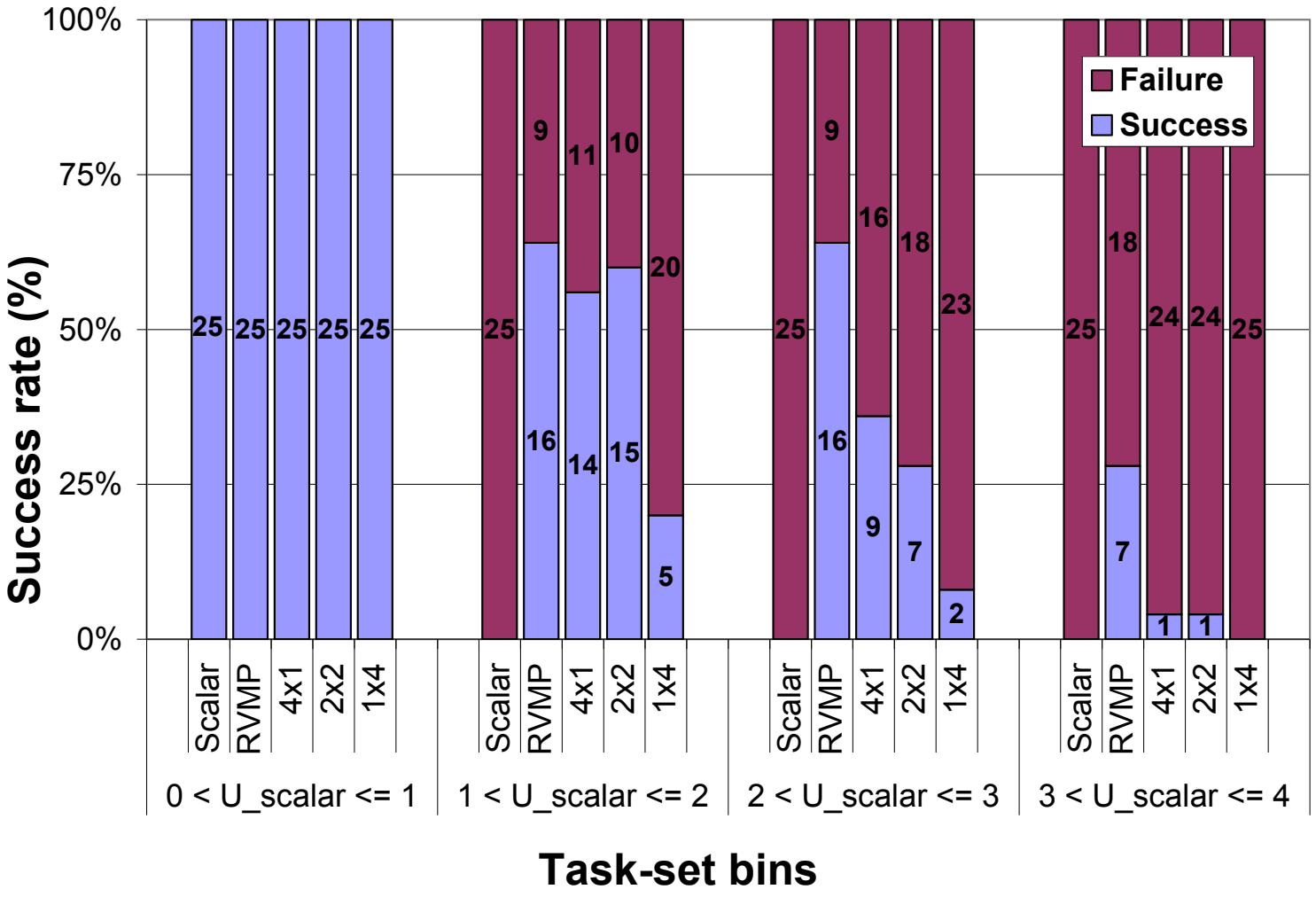
HRT

LTC	FV	PV	CVs	EOT
60			FU0  FU1  FU2  FU3  FU4 	0
40			FU0  FU1  FU2  FU3  FU4 	1
INVALID				
INVALID				

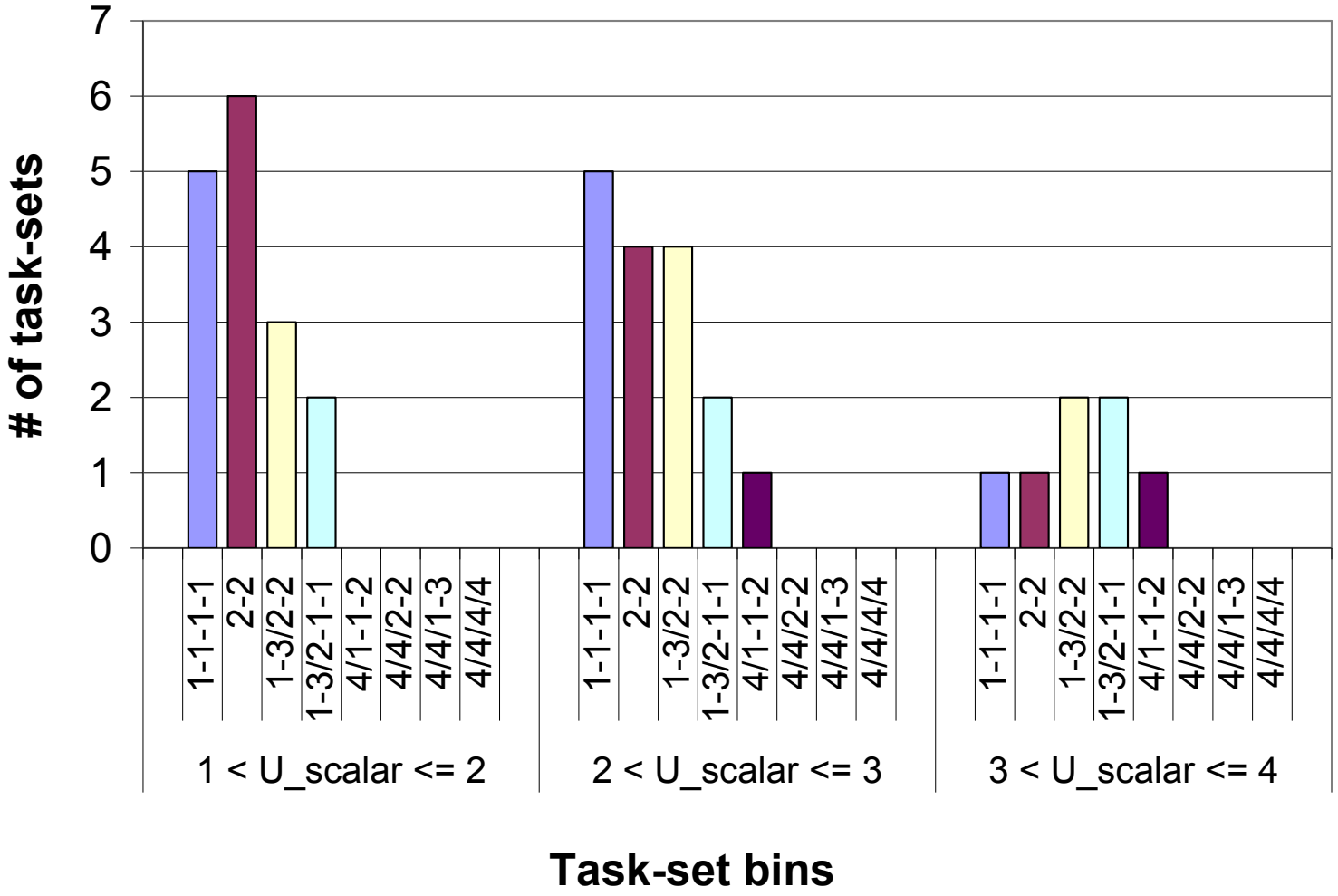
Experiments

- Tasks from C-lab and MiBench benchmarks
- 100 task-sets
  - 4 tasks per task-set (also 8 tasks in paper)
  - grouped according to *scalar* utilization (U_scalar)
- Two experiments
  - Worst-case schedulability analysis
  - Run-time experiments

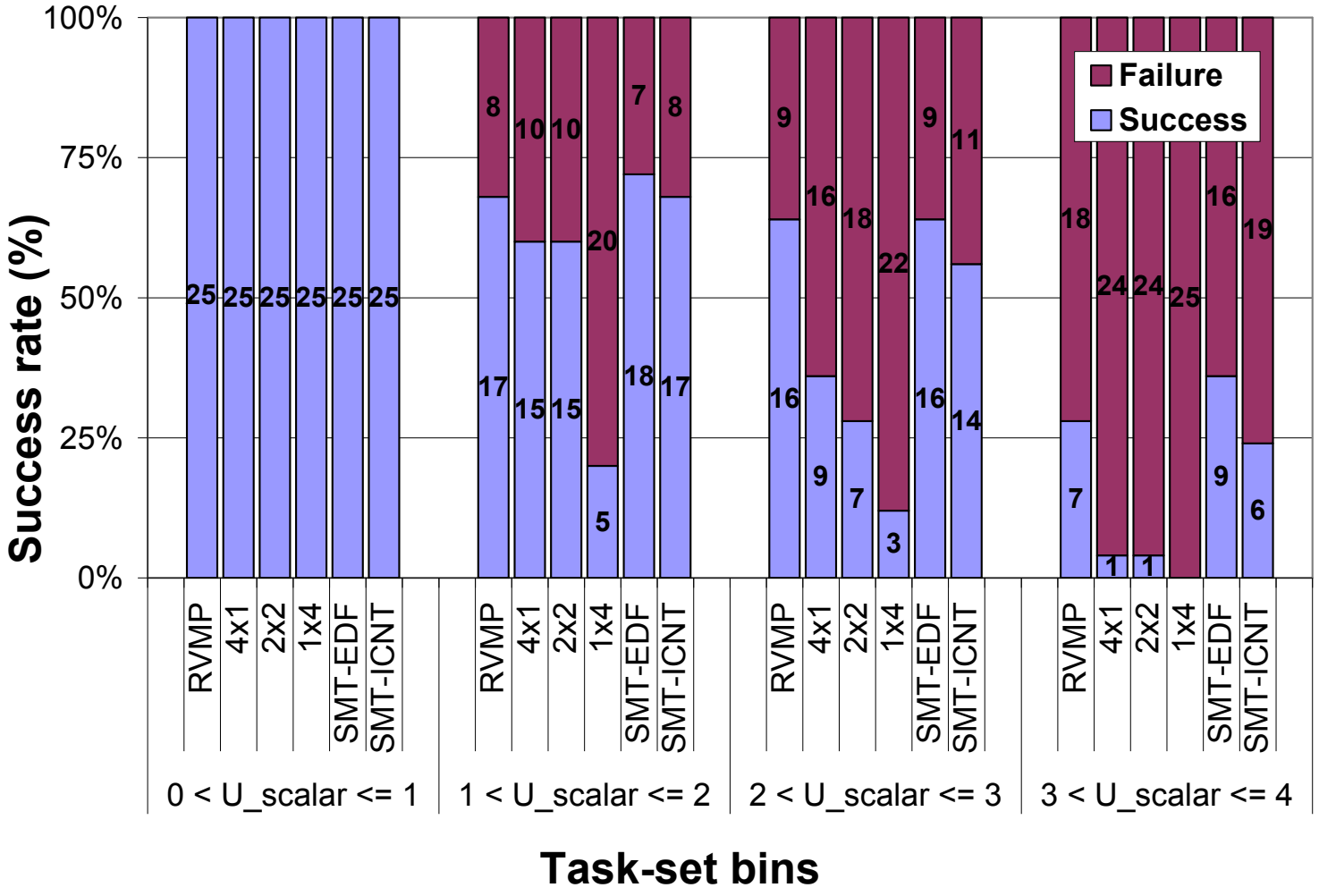
Worst-Case Schedulability Tests



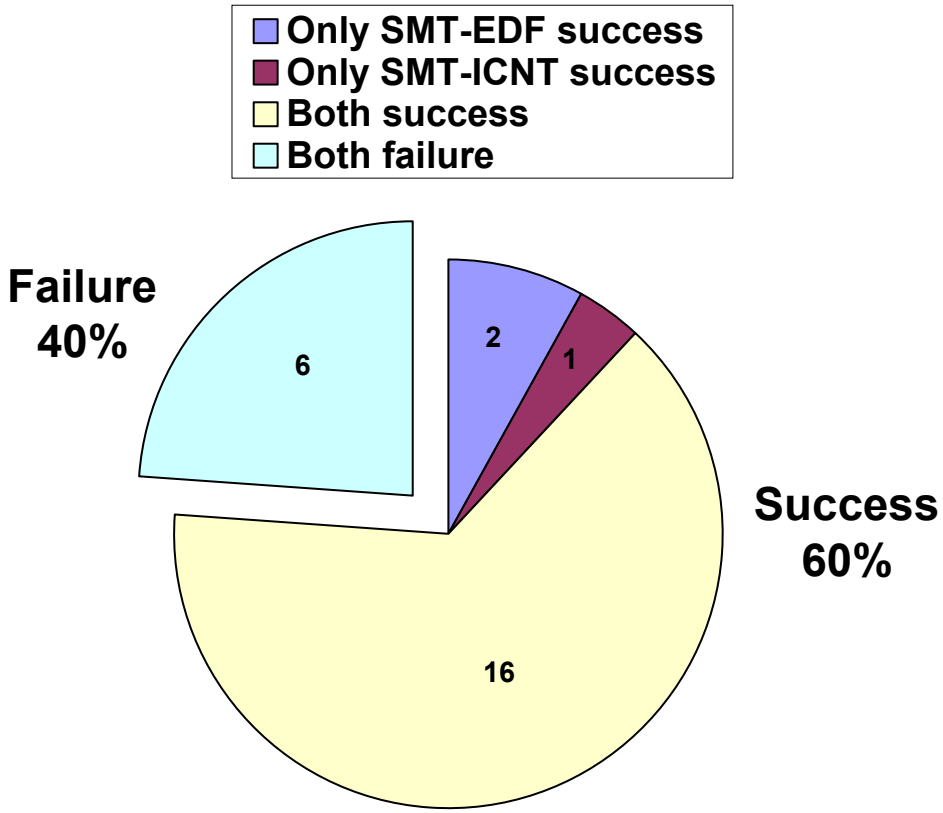
RVMP Configurations



Run-Time Experiments



Unsafe Behavior of SMT



1 < U_scalar <= 2

Summary

- Novel contributions
  - Virtualize a single processor
    - Space: variable-size interference-free partitions
    - Time: rapid reconfiguration
  - Simple real-time scheduling approach
- Analyzability of MP with flexibility of SMT
- Co-design processor and real-time scheduling for analyzable high-performance